Refine Search

09/927,803

Search Results -

Terms	Documents
L1 and (nonvolatile adj memory)	7

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L2

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Monday, December 29, 2003 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=ADJ			
L2	L1 and (nonvolatile adj memory)	7	L2
L1	DDD and LDD	205	L1

END OF SEARCH HISTORY

Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 7 of 7 returned.

☐ 1. Document ID: US 6071775 A

L2: Entry 1 of 7 File: USPT Jun 6, 2000

US-PAT-NO: 6071775
DOCUMENT-IDENTIFIER: US 6071775 A

TITLE: Methods for forming peripheral circuits including high voltage transistors with LDD structures

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWMC | Draw D

☐ 2. Document ID: US 6051465 A

L2: Entry 2 of 7 File: USPT Apr 18, 2000

US-PAT-NO: 6051465
DOCUMENT-IDENTIFIER: US 6051465 A

TITLE: Method for fabricating nonvolatile semiconductor memory device

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWMC | Draw D

☐ 3. Document ID: US 5917218 A

L2: Entry 3 of 7 File: USPT Jun 29, 1999

US-PAT-NO: 5917218
DOCUMENT-IDENTIFIER: US 5917218 A

TITLE: Peripheral circuits including high voltage transistors with LDD structures for nonvolatile memories

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWMC | Draw D

☐ 4. Document ID: US 5696006 A

L2: Entry 4 of 7 File: USPT Dec 9, 1997

US-PAT-NO: 5696006

DOCUMENT-IDENTIFIER: US 5696006 A

TITLE: Method of manufacturing Bi-MOS device

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 5. Document ID: US 5691556 A

L2: Entry 5 of 7 File: USPT Nov 25, 1997

US-PAT-NO: 5691556
DOCUMENT-IDENTIFIER: US 5691556 A

TITLE: Step-up semiconductor integrated circuit and electronic equipment using the semiconductor integrated circuit

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 6. Document ID: US 5641696 A

L2: Entry 6 of 7 File: USPT Jun 24, 1997

US-PAT-NO: 5641696
DOCUMENT-IDENTIFIER: US 5641696 A

TITLE: Method of forming diffusion layer and method of manufacturing nonvolatile semiconductor memory device

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 7. Document ID: US 5317179 A

L2: Entry 7 of 7 File: USPT May 31, 1994

US-PAT-NO: 5317179
DOCUMENT-IDENTIFIER: US 5317179 A

TITLE: Non-volatile semiconductor memory cell

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Terms	Documents
L1 and (nonvolatile adj memory)	7

Display Format: TI Change Format

Previous Page Next Page Go to Doc#

Refine Search

Search Results -

Terms	Documents
L3 and overlaps	8

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L4

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Monday, December 29, 2003 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=ADJ			
L4	L3 and overlaps	8	L4
L3	L1 and sacrificial	20	L3
L2	L1 and (nonvolatile adj memory)	7	L2
L1	DDD and LDD	205	L1

END OF SEARCH HISTORY

Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 8 of 8 returned.

☐ 1. Document ID: US 5949105 A

L4: Entry 1 of 8 File: USPT Sep 7, 1999

US-PAT-NO: 5949105
DOCUMENT-IDENTIFIER: US 5949105 A

TITLE: Insulated-gate field-effect transistor structure and method

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 2. Document ID: US 5834352 A

L4: Entry 2 of 8 File: USPT Nov 10, 1998

US-PAT-NO: 5834352
DOCUMENT-IDENTIFIER: US 5834352 A

TITLE: Methods of forming integrated circuits containing high and low voltage field effect transistors therein

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 3. Document ID: US 5716861 A

L4: Entry 3 of 8 File: USPT Feb 10, 1998

US-PAT-NO: 5716861
DOCUMENT-IDENTIFIER: US 5716861 A

TITLE: Insulated-gate field-effect transistor structure and method

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 4. Document ID: US 5591652 A

L4: Entry 4 of 8 File: USPT Jan 7, 1997

US-PAT-NO: 5591652
DOCUMENT-IDENTIFIER: US 5591652 A

TITLE: Method of manufacturing flash memory with inclined channel region

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Ds

☐ 5. Document ID: US 5502321 A

L4: Entry 5 of 8 File: USPT Mar 26, 1996

US-PAT-NO: 5502321
DOCUMENT-IDENTIFIER: US 5502321 A

TITLE: Flash memory having inclined channel

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Ds

☐ 6. Document ID: US 5098866 A

L4: Entry 6 of 8 File: USPT Mar 24, 1992

US-PAT-NO: 5098866
DOCUMENT-IDENTIFIER: US 5098866 A

TITLE: Method for reducing hot-electron-induced degradation of device characteristics

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Ds

☐ 7. Document ID: US 4928156 A

L4: Entry 7 of 8 File: USPT May 22, 1990

US-PAT-NO: 4928156
DOCUMENT-IDENTIFIER: US 4928156 A

TITLE: N-channel MOS transistors having source/drain regions with germanium

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Ds

☐ 8. Document ID: US 4837173 A

L4: Entry 8 of 8 File: USPT Jun 6, 1989

US-PAT-NO: 4837173
DOCUMENT-IDENTIFIER: US 4837173 A

TITLE: N-channel MOS transistors having source/drain regions with germanium

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Ds

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Terms	Documents
L3 and overlaps	8

Display Format: TI Change Format

Previous Page Next Page Go to Doc#